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| EXAMINER | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/943,512 | OSONE ET AL. | |
| | Examiner | Art Unit | |
| | David E. Graybill | 2894 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *14-23 and 25-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-23 and 25-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *All drawings* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

In view of the newly discovered Hayasaka reference, and upon further consideration, the previously indicated allowability of claims 25, 27, 46 and 47 is withdrawn, and claims 25, 27, 46 and 47 are more properly further examined on their merits. Any resulting inconvenience to applicant is sincerely regretted.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following claim features must be shown or the feature(s) canceled from the claim(s):

Re claim 16: an area which is projected onto the multilayer wiring board, thereto, which falls within an area where only through holes are built in the multilayer wiring board.

Re claim 27: the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes occupy, but the first and second end emitter electrodes of each of said groups of said emitter electrodes protrude from the area which the through holes occupy.

Figure 11 is objected to because it should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the

application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings filed on 10-27-04 are objected to because they reverse the corrections to FIG. 10 made in the drawings filed on 2-17-04.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 14.

The drawings are objected to because, in FIG. 11, reference character 10 appears to refer to the wrong part.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be

renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 16, 18/16, 19/16, 34, 35 and 51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The undescribed subject matter is the following:

Re claim 16: an area which is projected onto the multilayer wiring board, thereto, which falls within an area where only through holes are built in the multilayer wiring board.

Re claim 27: the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes occupy, but the first and second end emitter electrodes of each of said groups of said emitter electrodes protrude from the area which the through holes occupy.

To further clarify, the language, "only through holes are built in the multilayer wiring board" is a negative limitation; and, any negative limitation or exclusionary proviso must have basis in the original disclosure. See Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation or drawing illustration is not basis for an exclusion.

In fact, in the specification, at page 18, line 28 to page 19, line 8, applicant discloses that the area which is projected onto the multilayer wiring board, thereto, falls within an area where more than only through holes 4, e.g., "a material," are built in the multilayer wiring board because applicant discloses that the through holes 4 are "filled with a material."

Claims 26, 48, 49 and 54 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The

claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The undescribed subject matter is the following:

Re claim 26: the through holes of the semiconductor substrate being located directly above the through holes of the semiconductor substrate.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18, 19, 21, 22, 25, 26, 27, 31-33, 39, 40-42, 46, 48, 49 and 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of the following is unclear:

Re claim 26: the through holes of the semiconductor substrate being located directly above the through holes of the semiconductor substrate.

There is insufficient antecedent basis for the following claim language:

Re claim 18: the through holes.

Re claim 19: the through holes.

Re claim 21: the through holes (last occurrence).

Re claim 22: the through holes (last occurrence).

Re claim 25: The semiconductor device.

Re claim 27: the through holes (last occurrence).

Re claim 31: the first and second main surfaces of the semiconductor substrate.

Re claim 32: the first and second main surfaces of the semiconductor substrate.

Re claim 33: said plated heat sink.

The following is a relative term of degree which renders the claim indefinite:

Re claim 27: good thermal conductivity.

In particular, the relative term of degree is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Similarly, the relative language is subjective, qualitative language setting no limit on the scope of what is invented, and there is no method to measure what meets the claim limitations and what does not meet the claim limitations. See *Halliburton Energy Servs. v. M-I LLC*, 514 F.3d 1244, 85 U.S.P.Q.2d 1654 (Fed. Cir. 2008).

Claims 26, 33, 48, 49 and 54 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis

of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. Also see: In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious). See also MPEP 2143.03 and 2173.06. In re STEELE, MILLS, AND LEIS, 134 USPQ 292 (C.C.P.A. 1962), "Our analysis of the claims indicates that considerable speculation as to meaning of the terms employed and assumptions as to the scope of such claims were made by the examiner and the board. We do not think a rejection under 35 U.S.C. 103 should be based on such speculations and assumptions." Ex parte Tanksley, 26 USPQ2d 1384 (Bd. Pat. App. & Int., "it has been indicated in several prior decisions that claims may be too indefinite to be examined with respect to the prior art." Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Int. 1990), "With regard to the examiner's rejection of appealed claims 2, 4, 7, 8 and 10 through 12 under 35 USC 102(b) as anticipated by Morawski, it is our view that since the appealed claims are indefinite and indeterminate in scope for the reasons stated *supra,* it is not possible to apply the prior art to these claims in deciding patentability without disregarding portions of the express wording of the claims and thus resorting to speculation and conjecture as to

the particular invention defined therein. We therefore will not sustain the examiner's rejection of the appealed claims under 35 USC 102(b)." Ex parte Oetiker, 23 USPQ2d 1651 (Bd. Pat. App. & Int. 1990), "claims 2 through 9, 11, 13 and 19 contain additional indefinite language which precludes us from applying the prior art in determining the question of obviousness." Ex parte Brummer, 12 USPQ2d 1653 (Bd. Pat. App. & Int. 1989), "The examiner also has rejected the claims as being obvious in view of the bicycle disclosed by Moscogiuri. However, as set forth above, no reasonably definite meaning can be ascribed to certain language in claim 9 and, in such a case, the subject matter does not become obvious, the claim becomes indefinite." Ex parte LEWIN, 140 USPQ 70 (Bd. Pat. App. & Int. 1963). In re Merat and Cochez, 186 USPQ 471 (C.C.P.A. 1975).

MPEP 2111.01 [R-5] Plain Meaning

I. THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS **>SUCH MEANING IS INCONSISTENT WITH< THE SPECIFICATION

**> Although< claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, 367 F.3d 1359, 1369, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004) (The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation >in light of the specification<.). This means that the words of the claim must be given their plain meaning unless **>the plain meaning is inconsistent with< the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed below); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004) (Ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context changes their meaning, are construed to mean exactly what they say. Thus, "heating the resulting batter-coated dough to a temperature in the range of about 400°F

to 850°F" required heating the dough, rather than the air inside an oven, to the specified temperature.). **

>II. IT IS IMPROPER TO IMPORT CLAIM LIMITATIONS FROM THE SPECIFICATION

"Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." Superguide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875, 69 USPQ2d 1865, 1868 (Fed. Cir. 2004). See also Liebel-Flarsheim Co. v. Medrad Inc., 358 F.3d 898, 906, 69 USPQ2d 1801, 1807 (Fed. Cir. 2004)(discussing recent cases wherein the court expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment);< E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) ("Interpretation of descriptive statements in a patent's written description is a difficult task, as an inherent tension exists as to whether a statement is a clear lexicographic definition or a description of a preferred embodiment. The problem is to interpret claims in view of the specification' without unnecessarily importing limitations from the specification into the claims."); Altiris Inc. v. Symantec Corp., 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003) (Although the specification discussed only a single embodiment, the court held that it was improper to read a specific order of steps into method claims where, as a matter of logic or grammar, the language of the method claims did not impose a specific order on the performance of the method steps, and the specification did not directly or implicitly require a particular order). See also paragraph *>IV.<, below. **>When< an element is claimed using language falling under the scope of 35 U.S.C. 112, 6th paragraph (often broadly referred to as means or step plus function language)**, the specification must be consulted to determine the structure, material, or acts corresponding to the function recited in the claim. In re Donaldson, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994) (see MPEP § 2181- § 2186). In In re Zletz, supra, the examiner and the Board had interpreted claims reading "normally solid polypropylene" and "normally solid polypropylene having a crystalline polypropylene content" as being limited to "normally solid linear high homopolymers of propylene which have a crystalline polypropylene content." The court ruled that limitations, not present in the claims, were improperly imported from the specification. See also In re Marosi, 710 F.2d 799, 218 USPQ 289 (Fed. Cir. 1983) ("Claims are not to be read in a vacuum, and limitations therein are to be interpreted in light of the specification in giving them their broadest reasonable interpretation'." 710 F.2d at 802, 218 USPQ at 292 (quoting In re Okuzawa, 537 F.2d 545, 548, 190 USPQ 464, 466 (CCPA 1976)) (emphasis in original). The court looked to the specification to construe "essentially free of alkali metal" as including unavoidable levels of impurities but no more.). Compare In re Weiss, 989 F.2d 1202, 26 USPQ2d 1885 (Fed. Cir. 1993) (unpublished decision - cannot be cited as precedent) (The claim related to an athletic shoe with cleats that "break away at a preselected level of force" and thus prevent injury to the wearer. The examiner rejected the claims over prior art teaching athletic shoes with cleats not intended to break off and rationalized that the cleats would break away given a high enough force. The court reversed the rejection stating that when interpreting a claim term which is ambiguous, such as "a preselected level of force", we must look to the specification for the meaning ascribed to that term by the inventor." The specification had defined "preselected level of force" as that level of force at which the breaking away will prevent injury to the wearer during athletic exertion.**)

*>III. < "PLAIN MEANING" REFERS TO THE ORDINARY AND CUSTOMARY MEAN-ING GIVEN TO THE TERM BY THOSE OF ORDINARY SKILL IN THE ART

"[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." Phillips v. AWH Corp., *>415 F.3d 1303, 1313<, 75 USPQ2d 1321>, 1326< (Fed. Cir. 2005) (en banc). Sunrace Roots Enter. Co. v. SRAM Corp., 336 F.3d 1298, 1302, 67 USPQ2d 1438, 1441 (Fed. Cir. 2003); Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc., 334 F.3d 1294, 1298 67 USPQ2d 1132, 1136 (Fed. Cir. 2003)("In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art."). It is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the "ordinary" and the "customary" meaning of the terms in the claims. Ferguson Beauregard /Logic Controls v. Mega Systems, 350 F.3d 1327, 1338, 69 USPQ2d 1001, 1009 (Fed. Cir. 2003) (Dictionary definitions were used to determine the ordinary and customary meaning of the words "normal" and "predetermine" to those skilled in the art. In construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in context, and the intrinsic record must always be consulted to identify which of the different possible dictionary meanings is most consistent with the use of the words by the inventor.); ACTV, Inc. v. The Walt Disney Company, 346 F.3d 1082, 1092, 68 USPQ2d 1516, 1524 (Fed. Cir. 2003) (Since there was no >express< definition given for the term "URL" in the specification, the term should be given its broadest reasonable interpretation >consistent with the intrinsic record< and take on the ordinary and customary meaning attributed to it by those of ordinary skill in the art; thus, the term "URL" was held to encompass both relative and absolute URLs.); and E-Pass Technologies, Inc. v. 3Com Corporation, 343 F.3d 1364, 1368, 67 USPQ2d 1947, 1949 (Fed. Cir. 2003) (Where no explicit definition for the term "electronic multi-function card" was given in the specification, this term should be given its ordinary meaning and broadest reasonable interpretation; the term should not be limited to the industry standard definition of credit card where there is no suggestion that this definition applies to the electronic multi-function card as claimed, and should not be limited to preferred embodiments in the specification.). The ordinary and customary meaning of a term may be evidenced by a variety of sources, >including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art."< Phillips v. AWH Corp., *>415 F.3d at 1314<, 75 USPQ2d **>at 1327.< If extrinsic reference sources, such as dictionaries, evidence more than one definition for the term, the intrinsic record must be consulted to identify which of the different possible definitions is most consistent with applicant's use of the terms. Brookhill-Wilk 1, 334 F. 3d at 1300, 67 USPQ2d at 1137; see also Renishaw PLC v. Marposs Societa ' per Azioni, 158 F.3d 1243, 1250, 48 USPQ2d 1117, 1122 (Fed. Cir. 1998) ("Where there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meanings.") and Vitronics Corp. v. Conceptronic Inc., 90 F.3d 1576, 1583, 39 USPQ2d 1573, 1577 (Fed. Cir. 1996) (construing the term "solder reflow temperature" to mean "peak reflow temperature" of solder rather than the "liquidus temperature" of solder in order to remain consistent with the specification.). If more than one extrinsic definition is consistent with the use of the words in the intrinsic record, the claim terms may be construed to encompass all consistent meanings. ** See *>e.g.,< Rexnord Corp. v.

> Laitram Corp., 274 F.3d 1336, 1342, 60 USPQ2d 1851, 1854 (Fed. Cir. 2001)(explaining the court's analytical process for determining the meaning of disputed claim terms); Toro Co. v. White Consol. Indus., Inc., 199 F.3d 1295, 1299, 53 USPQ2d 1065, 1067 (Fed. Cir. 1999)("[W]ords in patent claims are given their ordinary meaning in the usage of the field of the invention, unless the text of the patent makes clear that a word was used with a special meaning."). Compare MSM Investments Co. v. Carolwood Corp., 259 F.3d 1335, 1339-40, 59 USPQ2d 1856, 1859-60 (Fed. Cir. 2001) (Claims directed to a method of feeding an animal a beneficial amount of methylsulfonylmethane (MSM) to enhance the animal's diet were held anticipated by prior oral administration of MSM to human patients to relieve pain. Although the ordinary meaning of "feeding" is limited to provision of food or nourishment, the broad definition of "food" in the written description warranted finding that the claimed method encompasses the use of MSM for both nutritional and pharmacological purposes.); and Rapoport v. Dement, 254 F.3d 1053, 1059-60, 59 USPQ2d 1215, 1219-20 (Fed. Cir. 2001) (Both intrinsic evidence and the plain meaning of the term "method for treatment of sleep apneas" supported construction of the term as being limited to treatment of the underlying sleep apnea disorder itself, and not encompassing treatment of anxiety and other secondary symptoms related to sleep apnea.).

The scope of the following language is unclear because the language is not clearly defined in the disclosure, and it otherwise has no plain meaning:

Re claim 21: an in-plane distribution.

Re claim 22: an in-plane distribution.

In the rejections infra, generally, reference labels and other claim element identifiers are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14-20, 31, 32 and 50-52 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hayasaka (6809421).

In a first particular interpretation of the instant claims and Hayasaka, at column 4, lines 12-14; column 7, lines 6-12 and 48-55; column 9, line 61 to column 10, line 7; column 10, lines 60-61; column 12, line 6 to column 13, line 8 to column 14, line 43; and column 28, lines 9-24 and 32-36; Hayasaka discloses the following:

Re claim 14: A multilayer wiring board 1c having "through holes" 13 in a thickness-wise direction, wherein a semiconductor substrate 1b mounted and superimposed on the multilayer wiring board has "through holes" 13 formed in a thicknesswise direction thererof, the through holes of the semiconductor substrate being located directly above the through holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 15: A multilayer wiring board 1c having "through holes" in a thickness-wise direction, wherein a semiconductor substrate 1b mounted and superimposed on the multilayer wiring board has "through holes"

formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly (i.e., in some measure or degree) overlap the through holes of the multilayer wiring board.

Re claim 16: A multilayer wiring board having a cross-plane through hole or holes, wherein an in-plane location of respective heat dissipating regions 13 in a semiconductor substrate mounted on the multilayer wiring board has an area which is projected onto the multilayer wiring board, perpendicular thereto, which falls within a through hole 13 or an area where only through holes 13 are built in the multilayer wiring board.

Re claim 17: A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows inherently one-dimensionally (at least) through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in

the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 18: The multilayer wiring board according to one of claims 14 to 16, wherein conductive layers 4 are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

Re claim 19: The multilayer wiring board according to one of claims 14 to 16, wherein a semiconductor element 1b is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

Re claim 20: The multilayer wiring board according to claim 14, wherein wirings 19a, 19b, 20a, 20b, which inherently connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

Re claim 31: A multilayer wiring board according to claim 15, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 32: A multilayer wiring board according to claim 14, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 50: The multilayer wiring board according to claim 14, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 51: The multilayer wiring board according to claim 16, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 52: The multilayer wiring board according to claim 17, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

MPEP 2112 [R-3] Requirements of Rejection Based on Inherency; Burden of Proof
V. ONCE A REFERENCE TEACHING PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS MADE THE BASIS OF A REJECTION, AND THE EXAMINER PRESENTS EVIDENCE OR REASONING TENDING TO SHOW INHERENCY, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE
"[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on inherency' under 35 U.S.C. 102, on prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. In re Fitzgerald, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977)).

MPEP 2112.01 [R-3] Composition, Product, and Apparatus Claims
I. PRODUCT AND APPARATUS CLAIMS — WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT
Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). "When the PTO shows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." In re Spada, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). Therefore, the prima facie case can be rebutted by evidence showing that the prior art products do not necessarily possess the characteristics of the claimed product.

MPEP 2113 [R-1] Product-by-Process Claims
ONCE A PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS FOUND AND A 35 U.S.C. 102 /103 REJECTION MADE, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE
"The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. In re Fessmann, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product.

MPEP 2114 [R-1] Apparatus and Article Claims — Functional Language
For a discussion of case law which provides guidance in interpreting the functional portion of means-plus-function limitations see MPEP § 2181 - § 2186.
APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE FROM THE PRIOR ART
>While features of an apparatus may be recited either structurally or functionally, claims<directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see

> also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

For reasons additional to the explicit disclosures supra, the structure and composition of the invention of Hayasaka appears to have the following inherent characteristics:

Re claim 17: heat flows inherently one-dimensionally (at least) through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board.

Re claim 20: wirings 19a, 19b, 20a, 20b, which inherently connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

In particular, because the **claimed** structure and composition and the structure and composition of Hayasaka are at least substantially identical, and/or are produced by at least substantially identical processes, a prima facie case of anticipation has been established, and applicant is required to prove that the structure of Hayasaka does not necessarily or inherently possess the characteristics of the instant claimed structure.

Claims 16, 18, 19, 21, 22, 34 and 51 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by applicant's admitted prior art.

In a second particular interpretation of the instant claims and applicant's admitted prior art, applicant admits as prior art the following:

Re claim 16: A multilayer wiring board 3 having a cross-plane through hole or holes 4, wherein an in-plane location "back surface of the device" of respective heat dissipating regions 5 in a semiconductor substrate 1 mounted on the multilayer wiring board has an area which is projected onto the multilayer wiring board, perpendicular thereto, which falls within a through hole or an area (area of the board abutting the semiconductor substrate in-plane location illustrated in FIG. 3, not labeled) where only through holes are built in the multilayer wiring board.

Re claim 18: The multilayer wiring board according to claim 16, wherein conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a "conductive" "material".

Re claim 19: The multilayer wiring board according to claim 16, wherein a semiconductor element 1 is mounted, in which conductive layers "gold plating" are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

Re claim 21: A multilayer wiring board having cross-plane through holes, wherein the through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: A multilayer wiring board having cross-plane through holes, wherein the through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of large and small cross-section areas of the through holes.

Re claim 34: A multilayer wiring board according to claim 16, wherein said semiconductor substrate includes emitter electrodes 7 located on a first main surface of the semiconductor substrate and a plated heat sink 6 located on a second main surface of the semiconductor substrate, opposite

to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 51: The multilayer wiring board according to claim 16, wherein said cross plane through hole or holes extend in the direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area (area of the board abutting the semiconductor substrate in-plane location illustrated in FIG. 3, not labeled) within the XY plane of a corresponding through hole or through holes of the multilayer wiring board.

For reasons additional to the explicit disclosures supra, the structure and composition of the invention of applicant's admitted prior art appears to have the following inherent characteristics:

Re claim 21: inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is

substantially identical with an in-plane distribution of large and small cross-section areas of the through holes.

In particular, because the **claimed** structure and composition and the structure and composition of applicant's admitted prior art are at least substantially identical, and/or are produced by at least substantially identical processes, a prima facie case of anticipation has been established, and applicant is required to prove that the structure of the admitted prior art does not necessarily or inherently possess the characteristics of the instant claimed structure.

Also, the following are statements of intended use:

Re claim 21: inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of large and small cross-section areas of the through holes.

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed structure and the structure of applicant's admitted prior art. Further, because the product of applicant's admitted prior art appears to have the same structure as the claimed structure, it appears to be capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed structure from the structure of the admitted prior art. In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (Court held that the purpose or intended use of hair curling was of no significance to the structure and process of making). The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And,

"Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)).

To further clarify, 37 CFR 1.84(p)(4) states:

> The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.

Therefore, as confirmed by applicant in the specification, at page 21, lines 7-10, identical reference characters of the instant invention and applicant's admitted prior art designate the same part.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-23, 25, 27-32, 34-47 and 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Hayasaka (6809421).

In a third particular interpretation of the instant claims and applicant's admitted prior art, the admitted prior art discloses all of the claim limitations except for the relative, overlapping locations of the semiconductor substrate 1 through holes 5 and wiring board 3 through holes 4 which results in the claimed heat dissipating function of the claimed product.

Nonetheless, Hayasaka discloses the claimed relative overlapping locations of the semiconductor substrate 1 through holes 4 and wiring board 3 through holes 5 which, in the obvious combination with the applied prior art, results in the claimed heat dissipating function of the claimed product.

Specifically, at page 10, lines 19-24; page 11, lines 12-17; page 12, line 1 to page 16, line 22; page 19, line 24 to page 20, line 8; and page 26, lines 10-17, applicant admits as prior art the following:

Re claim 14: A multilayer wiring board 3 having through holes 4 in a thickness-wise direction, wherein a semiconductor substrate 1 mounted and superimposed on the multilayer wiring board has through holes 5 formed in a thicknesswise direction thererof, the through holes of the semiconductor substrate being located above the through holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the multilayer wiring board.

Re claim 15: A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted and superimposed on the multilayer wiring board has through holes formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located respectively above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer

wiring board, perpendicular thereto, which partly (i.e., in some measure or degree) overlap the multilayer wiring board.

Re claim 16: A multilayer wiring board 3 having a cross-plane through hole or holes 4, wherein an in-plane location of respective heat dissipating regions 5 in a semiconductor substrate 1 mounted on the multilayer wiring board has an area which is projected onto the multilayer wiring board, perpendicular thereto, which falls within an area in the multilayer wiring board.

Re claim 17: A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows inherently one-dimensionally (at least) through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the multilayer wiring board.

Re claim 18: The multilayer wiring board according to one of claims 14 to 16, wherein conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a "conductive" "material".

Re claim 19: The multilayer wiring board according to one of claims 14 to 16, wherein a semiconductor element is mounted, in which conductive layers "gold plating" are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

Re claim 20: The multilayer wiring board according to claim 14, wherein wirings 10, which connect "heating areas" in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

Re claim 21: A multilayer wiring board having cross-plane through holes, wherein the through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: A multilayer wiring board having cross-plane through holes, wherein the through holes are distributed in the multilayer wiring board inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of large and small cross-section areas of the through holes.

Re claim 23: A multilayer wiring board, wherein a semiconductor substrate having cross-plane through holes, which are connected to emitter wirings 10 connected to "emitters" of heterojunction bipolar transistors "HBTs" and extended through the semiconductor substrate and which have conductive layers "gold plating" on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the cross-plane through holes in the semiconductor substrate and through holes extending through the multilayer wiring board are connected to each other, and wherein conductive layers "gold plating" "conductive" "material" are provided on sides of or inside of the connected through holes in the semiconductor substrate and the multilayer wiring board, and the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the multilayer wiring board.

Re claim 25: The semiconductor device including a plurality of "finger"-shaped emitter electrodes 7 or source electrodes, and at least one via hole 5 which are arranged in rows in a first direction on a semiconductor substrate, wherein the emitter electrodes or the source electrodes are connected to a conductive layer 6 formed on a back surface opposite to a surface, on which the electrodes are formed, through the via hole, and wherein said rows comprising the emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally shifted from one another ("in a longitudinal direction in the figure [FIG. 11]") in adjacent rows among said rows, or adjacent rows are positionally shifted from one another in the first direction, wherein a multilayer wiring board has through holes formed on sides thereof or inside thereof with a conductive layer, and areas, which the via holes of the semiconductor device occupies, overlap areas which the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

Re claim 27: A multilayer wiring board having through holes, wherein emitter electrodes of heterojunction bipolar transistors are arranged in line on a semiconductor substrate, said semiconductor substrate is mounted on said multilayer wiring board, and said multilayer wiring board has cross-plane through holes, said through holes in the multilayer wiring board having

on sides or inside thereof a material of good thermal conductivity, wherein said emitter electrodes are arranged in a line to form "groups", such that all emitter electrodes in a group are connected with a common emitter wiring 10, wherein each group includes central emitter electrodes located between first and second end emitter electrodes, wherein said first and second end emitter electrodes are located, respectively, at opposite ends of the central emitter electrodes, and wherein, with respect to a positional relation viewed from a normal direction to an in-plane surface of said multilayer wiring board, the central emitter electrodes in each of said groups of said emitter electrodes are included in an area.

Re claim 28: A multilayer wiring board according to claim 14, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink 6 located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 29: A multilayer wiring board according to claim 28, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 30: A multilayer wiring board according to claim 29, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer 2.

Re claim 31: A multilayer wiring board according to claim 15, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 32: A multilayer wiring board according to claim 14, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 34: A multilayer wiring board according to claim 16, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 35: A multilayer wiring board according to claim 34, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 36: A multilayer wiring board according to claim 17, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located

on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 37: A multilayer wiring board according to claim 36, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 38: A multilayer wiring board according to claim 37, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 39: A multilayer wiring board according to claim 21, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 40: A multilayer wiring board according to claim 39, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 41: A multilayer wiring board according to claim 22, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located

on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 42: A multilayer wiring board according to claim 41, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 43: A multilayer wiring board according to claim 23, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 44: A multilayer wiring board according to claim 43, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

Re claim 45: A multilayer wiring board according to claim 44, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 46: A multilayer wiring board according to claim 25, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located

on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

Re claim 47: A multilayer wiring board according to claim 46, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

Re claim 50: The multilayer wiring board according to claim 14, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of the multilayer wiring board.

Re claim 51: The multilayer wiring board according to claim 16, wherein said cross plane through hole or holes extend in the direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area within the XY plane of the multilayer wiring board.

Re claim 52: The multilayer wiring board according to claim 17, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of the multilayer wiring board.

Re claim 53: The multilayer wiring board according to claim 23, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of the multilayer wiring board.

For reasons additional to the explicit disclosures supra, the structure and composition of the invention of applicant's admitted prior art appears to have the following inherent characteristics:

Re claim 17: heat flows inherently one-dimensionally (at least) through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board.

Re claim 21: inherently to be aligned relative to at least one "transistor" of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: inherently to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of large and small cross-section areas of the through holes.

In particular, because the **claimed** structure and composition and the structure and composition of applicant's admitted prior art are at least substantially identical, and/or are produced by at least substantially identical processes, a prima facie case of anticipation has been established, and applicant is required to prove that the structure of the admitted prior art does not necessarily or inherently possess the characteristics of the instant claimed structure.

Also, the following are statements of intended use:

Re claim 21: to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially

identical with an in-plane distribution of large and small cross-section areas of the through holes.

Moreover, the statements of intended use do not appear to result in a structural difference between the claimed structure and the structure of applicant's admitted prior art. Further, because the product of applicant's admitted prior art appears to have the same structure as the claimed structure, it appears to be capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed structure from the structure of the admitted prior art. In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (Court held that the purpose or intended use of hair curling was of no significance to the structure and process of making). The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Also, "Expressions relating the apparatus to contents thereof during an intended

operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)).

However, applicant does not appear to explicitly admit as prior art the following:

Re claim 14: the through holes of the semiconductor substrate being located directly above the through holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 15: the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly overlap the through holes of the multilayer wiring board.

Re claim 16: the area which is projected onto the multilayer wiring board, perpendicular thereto, falls within a through hole or an area where only through holes are built in the multilayer wiring board.

Re claim 17: heat flows one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the

multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

Re claim 21: the through holes are distributed in the multilayer wiring board to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of the through holes.

Re claim 22: the through holes are distributed in the multilayer wiring board to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the transistor is substantially identical with an in-plane distribution of large and small cross-section areas of the through holes.

Re claim 23: the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes in the multilayer wiring board.

Re claim 25: areas, which the via holes of the semiconductor device occupies, overlap areas which the through holes of the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

Re claim 27: the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes occupy, but the first and second end emitter electrodes of each of said groups of said emitter electrodes protrude from the area which the through holes occupy.

Re claim 50: an entirety of each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 51: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area within the XY plane of a corresponding through hole or through holes of the multilayer wiring board.

Re claim 52: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Re claim 53: an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Nevertheless, as cited supra, Hayasaka discloses the through holes 13 of the semiconductor substrate 1b being located directly above the through holes 13 of the multilayer wiring board 1c, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board; the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which partly (i.e., in some measure or degree) overlap the through holes of the multilayer wiring board; the area which is projected onto the multilayer wiring board, perpendicular thereto, falls within a through hole or an area where only through holes are built in the multilayer wiring board; heat flows one-dimensionally (at least) through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the

semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board; the through holes are distributed in the multilayer wiring board to be aligned relative to at least one through hole of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the semiconductor substrate is substantially identical with an in-plane distribution of the through holes; the through holes are distributed in the multilayer wiring board to be aligned relative to at least one through hole of a semiconductor substrate mounted on the multilayer wiring board such that an in-plane distribution of heat dissipated from the semiconductor substrate is substantially identical with an in-plane distribution of large and small cross-section areas of the through holes; areas, which the via holes of the semiconductor device occupies, overlap areas which the through holes of the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board; and an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area within the XY plane of a corresponding through hole or through holes of the multilayer wiring board.

Moreover, it would have been obvious to combine this disclosure of Hayasaka with the disclosure of applicant's admitted prior art because it would facilitate heat dissipation from the product of the admitted prior art.

Also, in the above combination of applicant's admitted prior art and Hayasaka, the following claimed structure would inherently result:

Re claim 27: the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes occupy, but the first and second end emitter electrodes of each of said groups of said emitter electrodes protrude from the area which the through holes occupy.

To further clarify, when the central emitter electrodes 7 in each of said groups of emitter electrodes illustrated in the prior art FIG. 4 are combined with Hayasaka to be included in an area which said through holes occupy as illustrated in FIG. 2c, the first and second end emitter electrodes (illustrated in FIGS. 2c and 4, not individually labeled) of each of said groups of said emitter electrodes protrude from the area which the through holes occupy.

Applicant's amendment and remarks filed 3-26-08, 8-26-08 and 12-23-08 have been fully considered and are adequately treated in the rejections and objections supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

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**Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.**

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

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